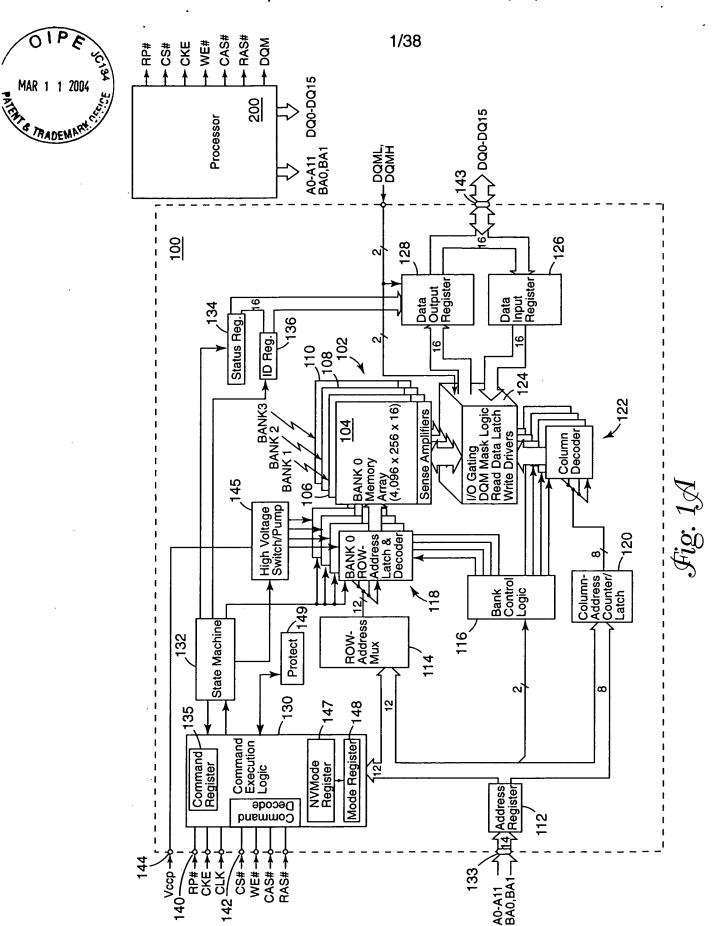
H OF







<u></u>		
Vcc III 1* DQ0 III 2	·	54
VccQ		52 🞞 VssQ
DQ1		51 🗀 DQ14
DQ2 🖽 5		50 🗀 DQ13
VssQ Ⅲ 6	<u>150</u>	49 🖽 VccQ
DQ3 田 7		48 <u>DQ12</u>
DQ4 III 8		47 DQ11
VccQ III 9		46 ⊞ VssQ 45 ⊞ DQ10
DQ5 🖽 10 DQ6 🖽 11		45 ⊞ DQ10 44 ⊞ DQ9
VssQ III 12		43 H VccQ
DQ7 🖽 13		42 DQ8
Vcc III 14		41 🗔 Vss
DQML III 15		40 \(\overline{RP#} \) 152
WE# Ⅲ 16		39 🎞 DQMH
CAS# 🎞 17		38 🞞 CLK
RAS# □ 18		37 🗆 CKE 154
CS# □ 19		36 □ VccP 154
BA0 🖽 20		35 E A11
BA1 III 21		34 <u> </u>
A10 III 22		33 H A8
A0 🖽 23 A1 🖽 24		32
A1 🖽 24 A2 🖽 25		30 H A5
A3 🖽 26		29 H A4
Vcc = 27		28 H Vss
		/ <u>/</u>

Fig. 1B



0		
1 2		7 8
A (DQ15) (Vss)		(Vcc) (DQ0)
B (DQ14) (VssQ)	400	(Noo) (DO1)
B (DQ14) (VssQ)	<u>160</u>	(VccQ) (DQ1)
C (VccQ) (DQ13)		(DQ2) (VssQ)
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		
D (DQ11) (DQ12)		(DQ3) (DQ4)
E (DQ10) (VssQ)		(VccQ) (DQ5)
North North		
F (VccQ) (DQ9)		(DQ6) (VssQ)
G (NC) (DQ8)		(DQ7) (NC)
H (NC) (Vss)		(Vcc) DQML
J (NC) DOMH		(WE#) (CAS#)
J (NO) Edwill		WE# OAG#)
K (RP#) (CLK)		(RAS#) (NC)
L (VccP) (CKE)		(NC) (CS#)
L (VccP) (CKE)		NC (CS#)
M (A11) (A9)		(BA1) (BA0)
N (A8) (A7)		(A0) (A10)
P (A6) (A5)		(A2) (A1)
R (A4) (Vss)		(Vcc) (A3)
1		



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· · · · · · · · · · · · · · · · · · ·	<u> </u>
	tr 21
	Fig. 2A
·	
	Fig. 2B

Fig. 2



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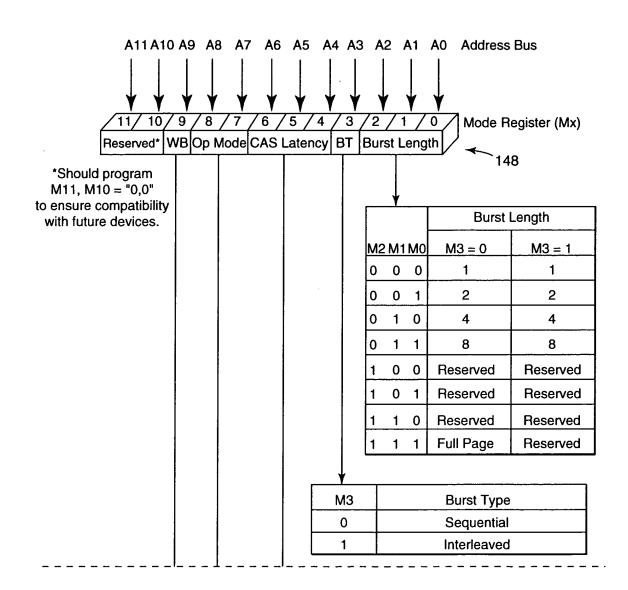


Fig. 2A



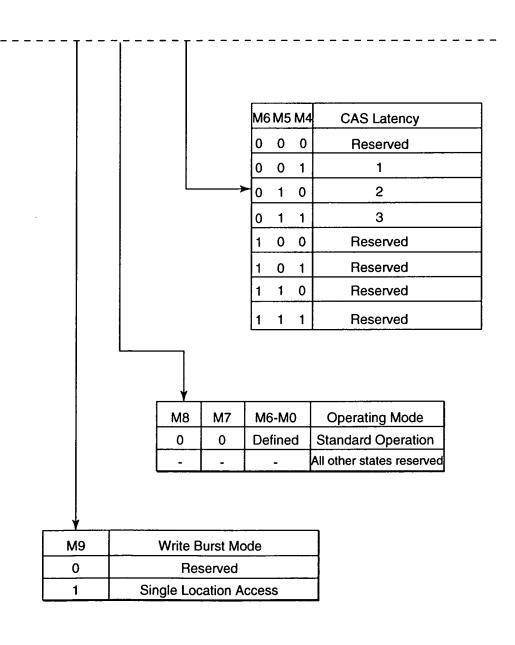


Fig. 2B

MAR 1 1 2004 TRADEN'

First Named Inventor: Frankie F. Roohparvar SYNCHRONOUS FLASH MEMORY WITH ACCESSIBLE PAGE DURING WRITE Atty Docket No. 400.044US01 Serial No. 09/627,770

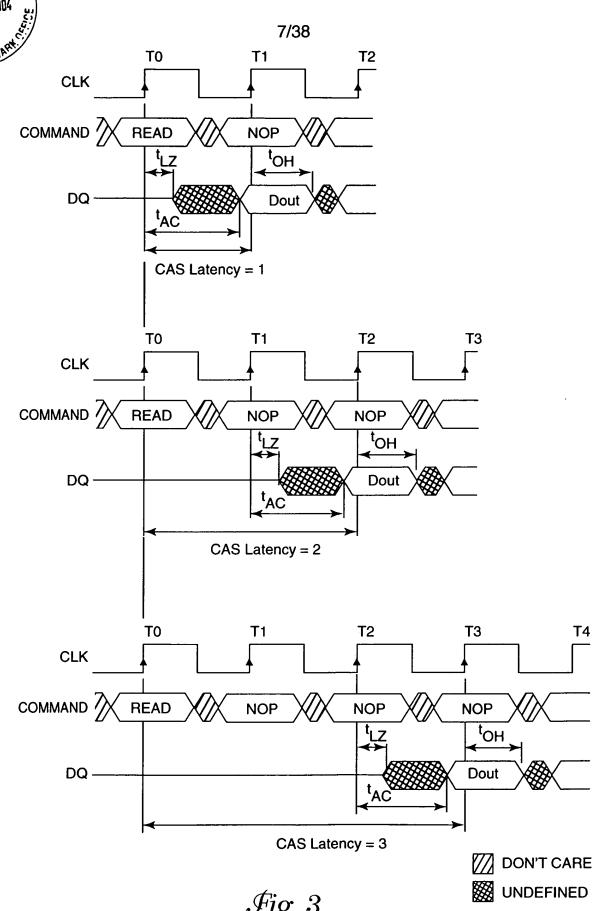


Fig. 3



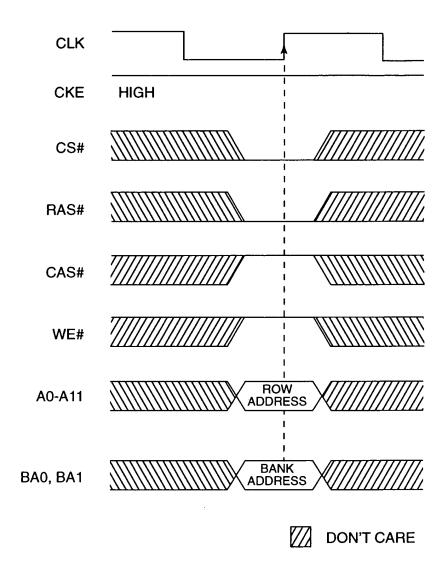
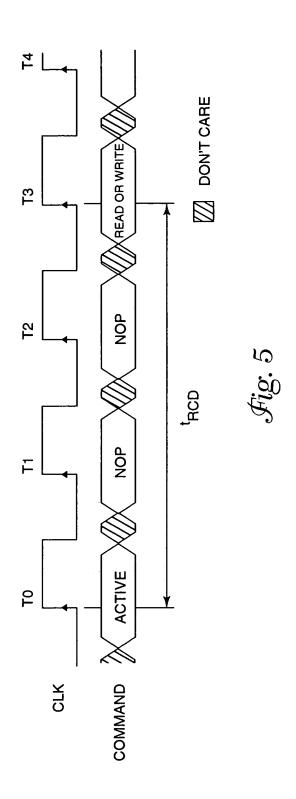


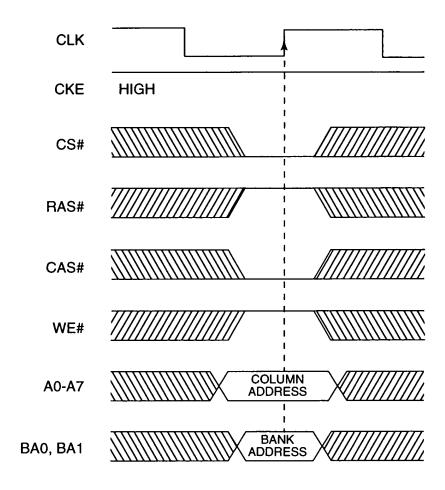
Fig. 4







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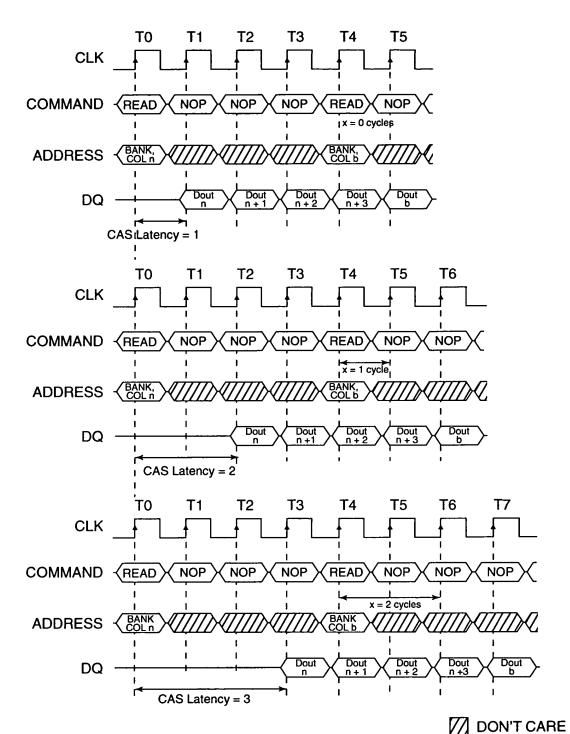


DON'T CARE

Fig. 6



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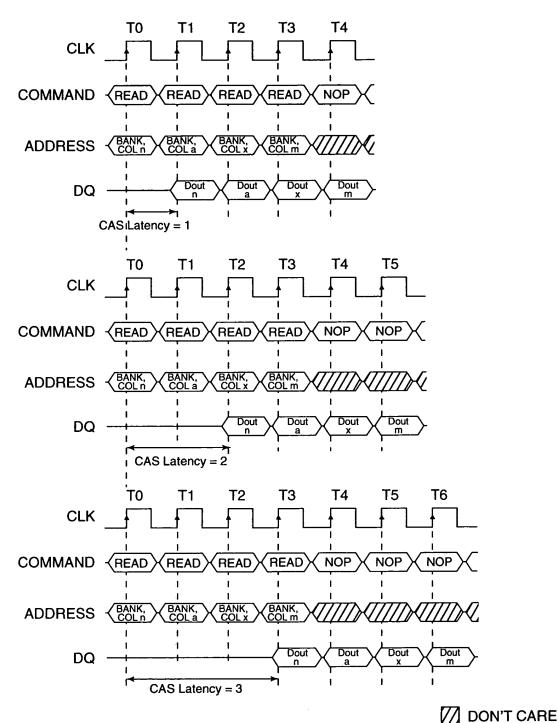


NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 7



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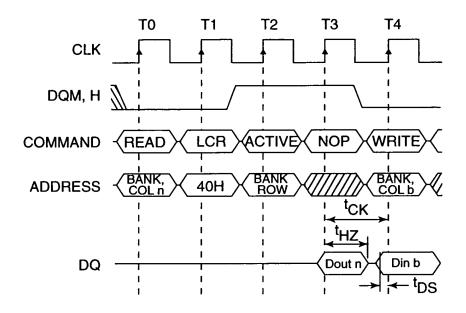


NOTE: Each READ command may be to either bank. DQM is LOW.

Fig. 8



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NOTE:

A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank. If a CAS latency of one is used, then DQM is not required.

DON'T CARE

Fig. 9



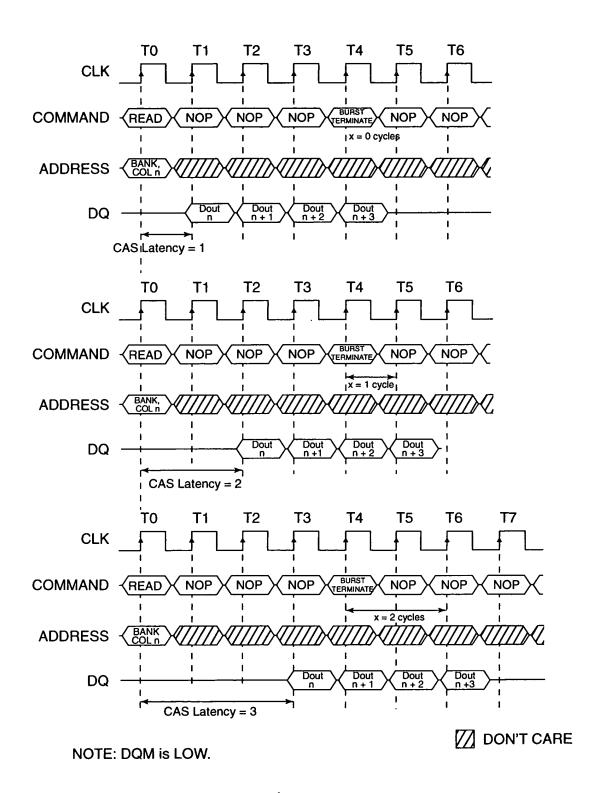


Fig. 10



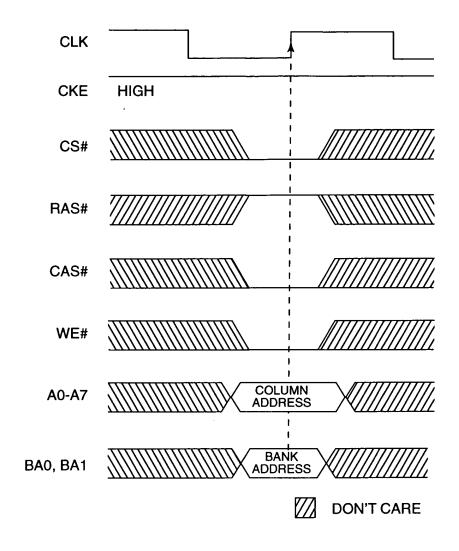
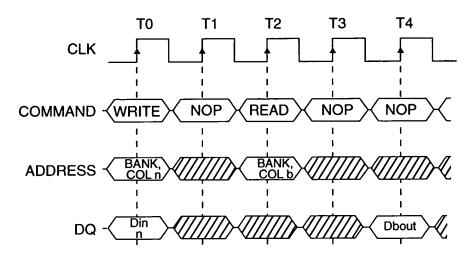


Fig. 11



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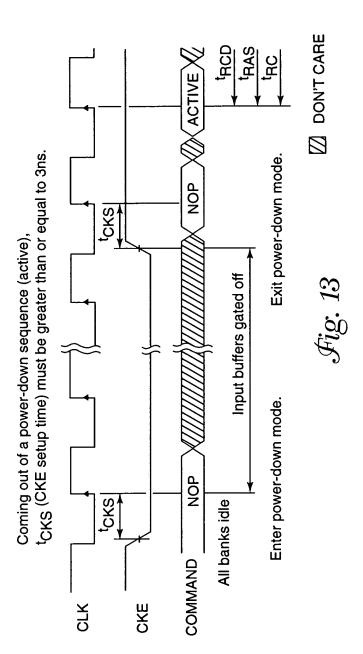


NOTE: A CAS latency of two is used for illustration. The WRITE command may be to any bank and the READ command may be to any bank. DQM is LOW. A READ to the bank undergoing the WRITE ISM operation may output invalid data.

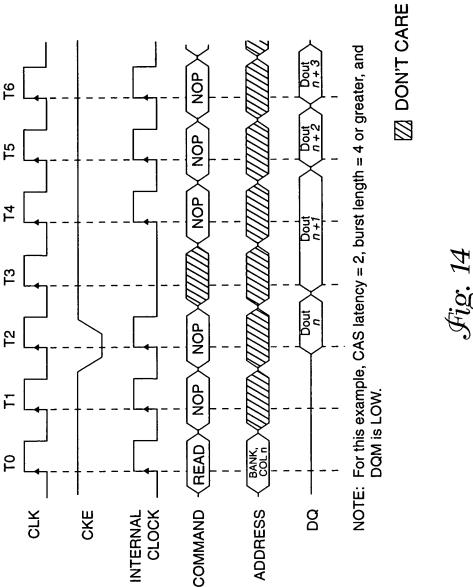
DON'T CARE

Fig. 12











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ADDRESS RANGE

	\$	arix Pr	on Col	right.	
	3	FFF C00	FFH 00H	256K-Word Block 15	210
k 3	ფფფფფფფ ფ	BFF 800	FFH 00H	256K-Word Block 14]
Bank 3	3 3	7FF 400	FFH 00H	256K-Word Block 13	
	3 3	3FF 000	FFH 00H	256K-Word Block 12	
	2	FFF C00	FFH 00H	256K-Word Block 11]
k 2	2	BFF 800	FFH 00H	256K-Word Block 10	
Bank 2	7FF 400	FFH 00H	256K-Word Block 9		
	3FF 000	FFH 00H	256K-Word Block 8		
	1	FFF C00	FFH 00H	256K-Word Block 7	
k 1	l ilă	BFF 800	FFH 00H	256K-Word Block 6	
Bank 1	7FF 400	FFH 00H	256K-Word Block 5		
		3FF 000	FFH 00H	256K-Word Block 4	
	0	FFF C00	FFH 00H	256K-Word Block 3	
6 A	. 0	BFF 800	FFH 00H	256K-Word Block 2	
Bank 0	0	7FF 400	FFH 00H	256K-Word Block 1	220
	0 0	3FF 000	FFH 00H	256K-Word Block 0	

Word-wide (x16)

Software Lock = Hardware-Lock Sectors
RP# = Vhh to unprotect if either the
block protect or device protect bit is set.

Software Lock = Hardware-Lock Sectors
RP# = Vcc to unprotect but must be VHH
if the device protect bit is set.

See BLOCK PROTECT/UNPROTECT SEQUENCE for detailed information.

Fig. 15



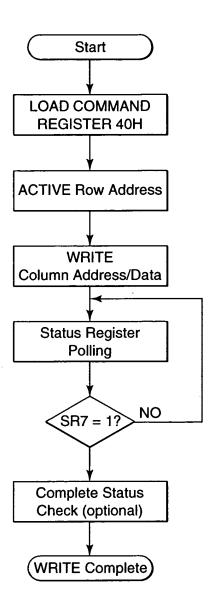


Fig. 16



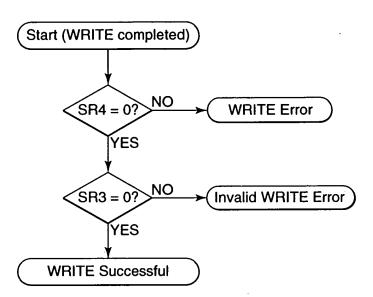


Fig. 17



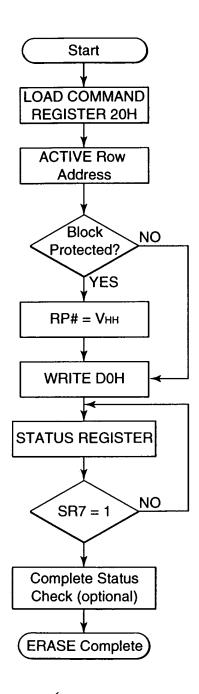


Fig. 18



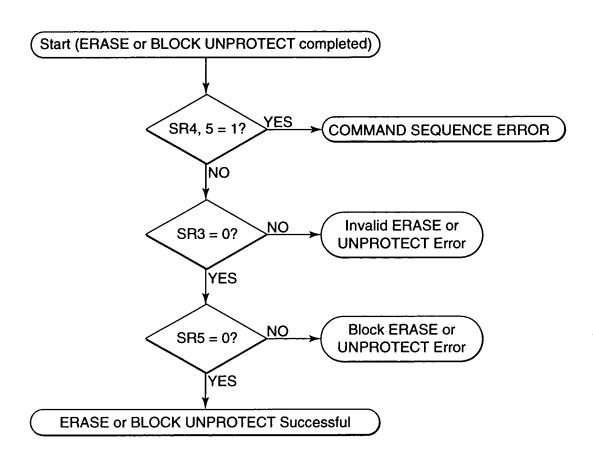


Fig. 19



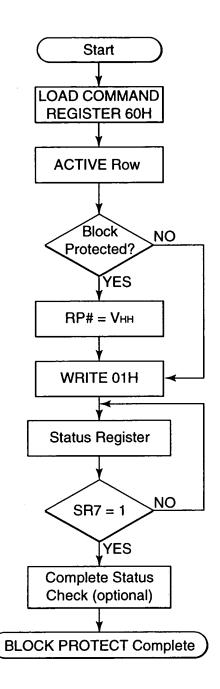


Fig. 20



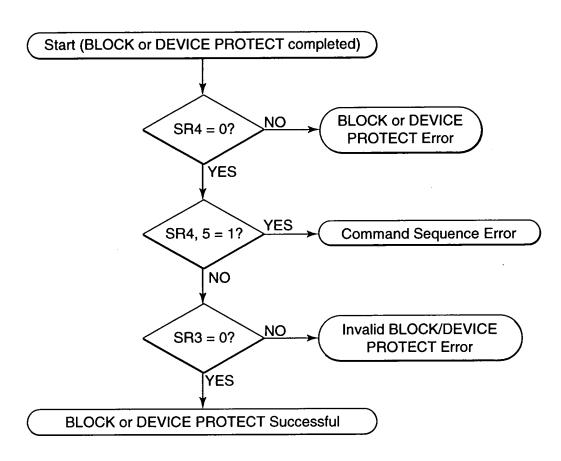


Fig. 21



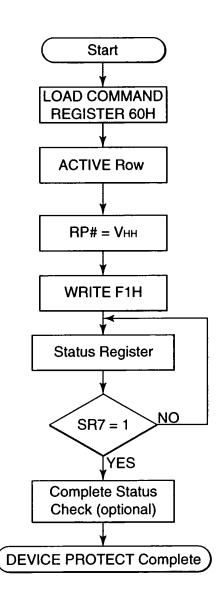


Fig. 22



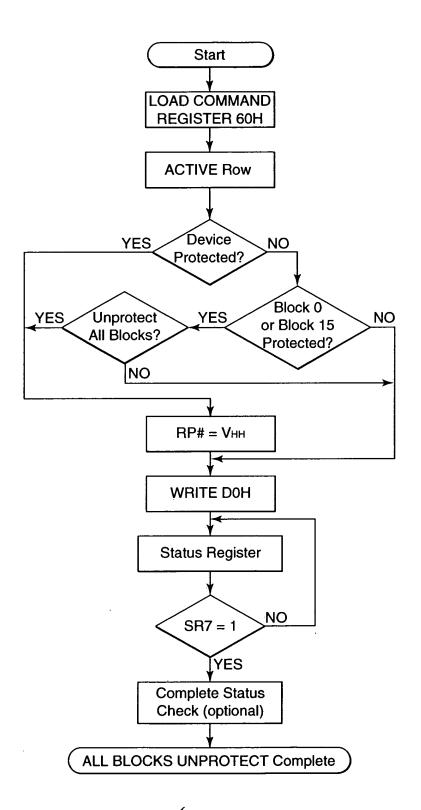


Fig. 23



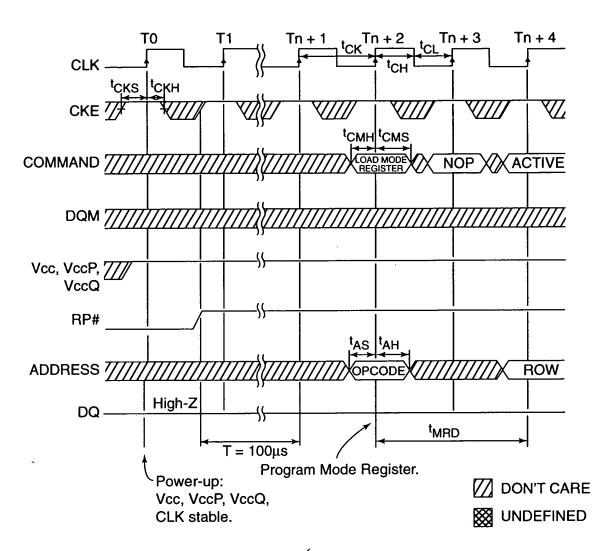
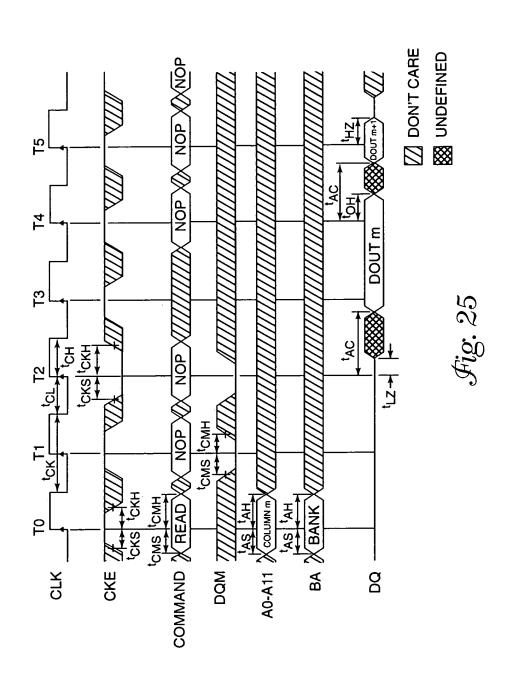
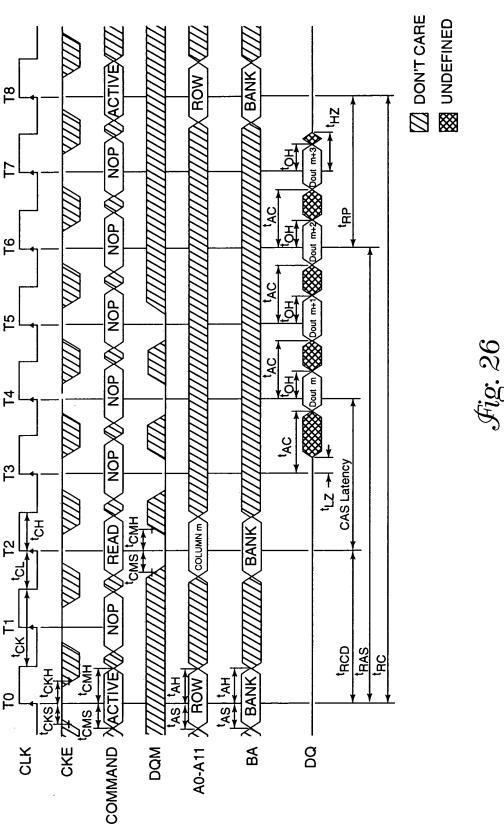


Fig. 24

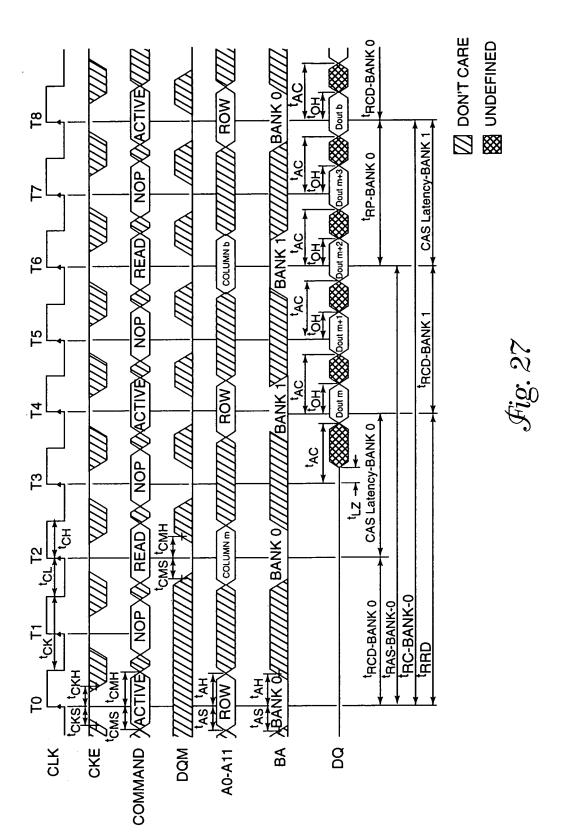




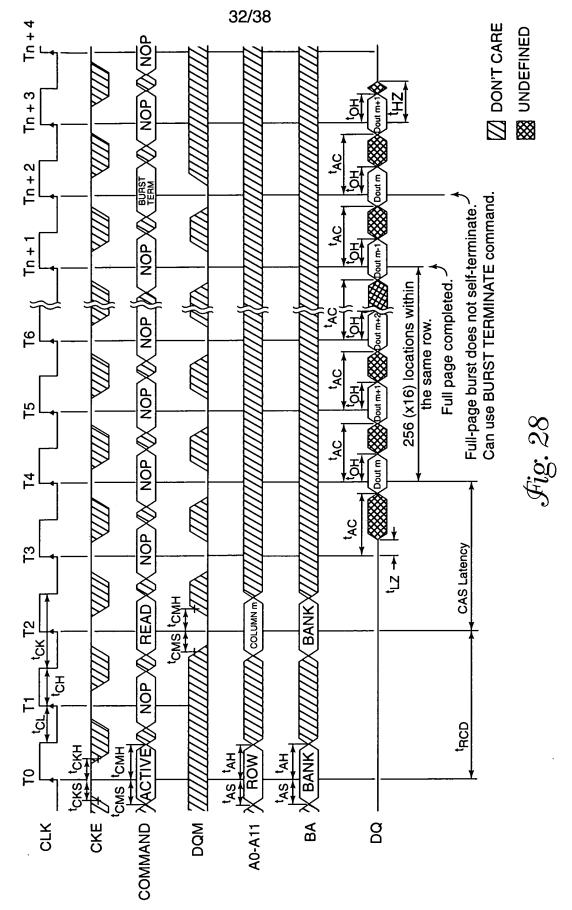




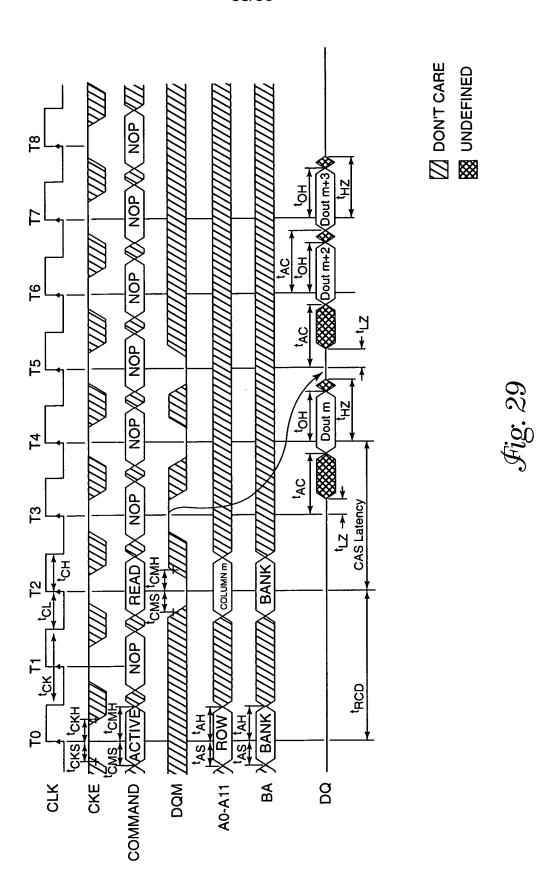




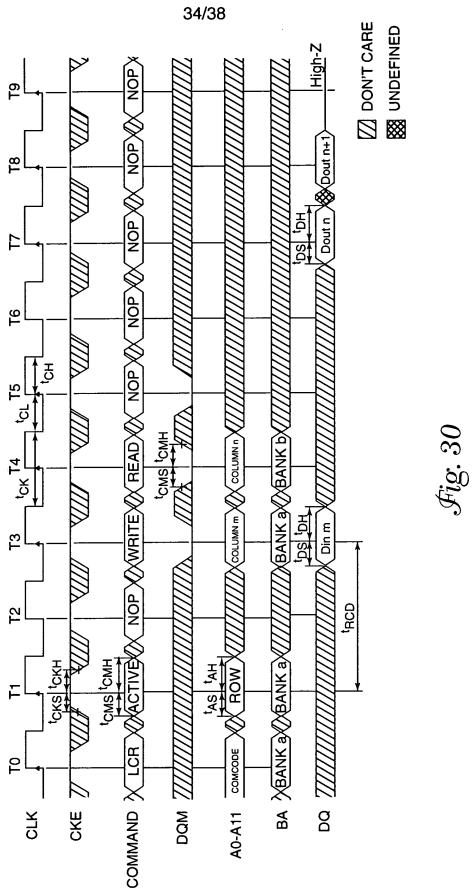




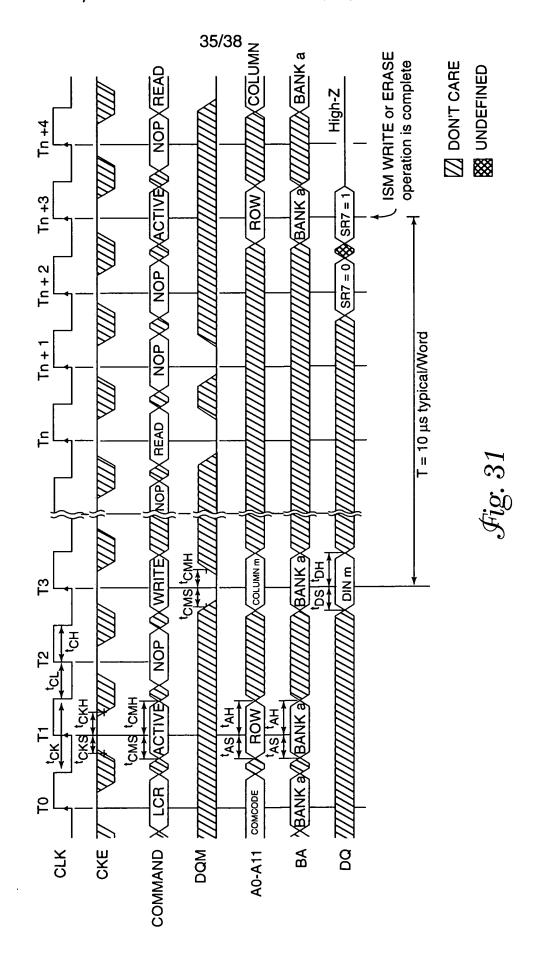














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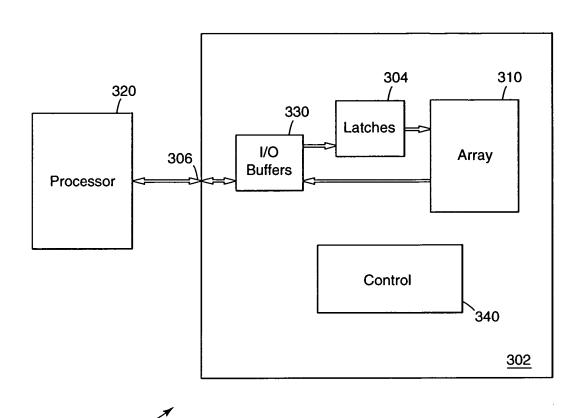
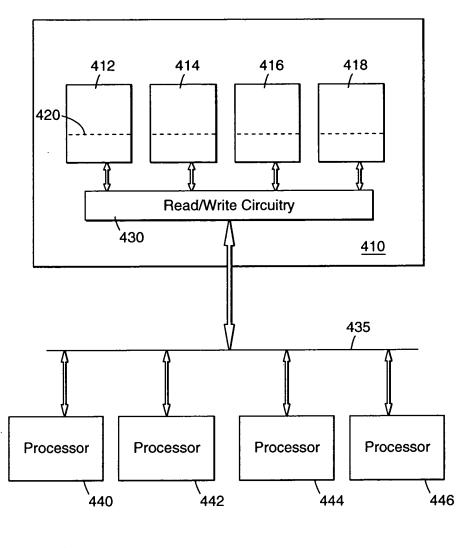


Fig. 32

300





400 Fig. 33



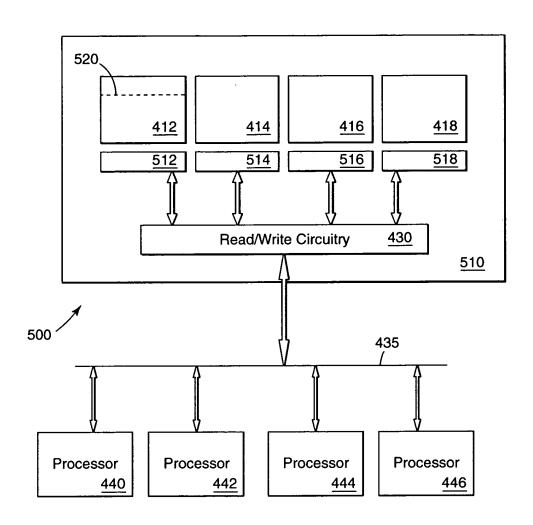


Fig. 34